ABSTRACT

A DC converter with a halt mode setting is disclosed for preventing the occurrence of over-current while alleviating the increase in the size of circuits, along with a method for setting up such a halt mode. The DC converter includes a semiconductor switch, a clock generator for outputting a clock signal to a gate of the semiconductor switch to be utilized for controlling an on/off time of the semiconductor switch such that a predetermined power is output from the generator, and a drive circuit for switching the semiconductor switch to the continuous-on state according to a halt mode setting requirement regardless of the clock signal, when the semiconductor switch, normally repeating on/off operations responsive to the clock signal, is in its off-state.